ALPHA DATA

ADA-VPX3-7K1
User Manual

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1 Overview

1.1 Introduction

The ADA-VPX3-7K1 is a high-performance VPX card based around the Xilinx™ Kintex-7 FPGA. This card supports XC7K325T and KC7K410T devices in the FFG900/FBG900 package.

Xilinx™ Kintex-7 devices are the mid-range of Xilinx™'s three-tier 7-Series FPGA family, offering a balance between power consumption and performance.

The ADA-VPX3-7K1 includes a separate FPGA with a PCIe bridge developed by Alpha Data. This guarantees a ready-made data channel capable of transferring 2GB/s in each direction between the board's host interface and the target FPGA. The bridge FPGA relieves the user of the need to integrate a propierty core, such as a PCIe endpoint, in their FPGA design. The fixed design in the bridge FPGA allows the board to be immediately identified on the PCI bus by the host system and in turn recognised by the Alpha Data ADB3 Device Driver. This exposes a set of C API calls, enabling the user to easily peform tasks such as configuring the target FPGA and transferring data in and out of the FPGA.

The ADA-VPX3-7K1 is targeted for use in military and commercial rugged 3U VPX Systems. It is fully compliant with multiple OpenVPX configurations delivering performance and flexibility through development and deployment.

1.2 Key Features

Key Features

- 3U OpenVPX, compliant to VITA Standard 46.0 and 65
- Dedicated 4-lane PCI-Express Gen 2 interface with high-performance DMA controllers
- Two VPX control planes connected to target FPGA
- VPX User I/O interface with 72 GPIO (single ended or differential) signals and up to 16 Multi-Gigabit (MGT) links
- Two mSATA sites linked to target FPGA
- Support for Kintex-7 FPGAs in FFG/FBG900 package
- 2 independent banks of DDR3-1600 SDRAM, 256MB/bank, 512MB total. Alternatively, 2 independent banks of DDR3-800 SDRAM, 512MB/bank, 1GB total
- Front-panel (XRM) interface with adjustable voltage, with 146 GPIO signals and potential for 8 GTX links to target FPGA (2 dip-switch selectable groups of 4 GTX links routed to either XRM or P6)
- On-board programmable clocks enabling multiple protocols to be implemented on the target FPGA's high-speed links
- Voltage and temperature monitoring
- Air-cooled and conduction-cooled configurations

Open VPX Compliance List

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F1F2U-14.2.4
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7
- SLT3-PAY-1F4U-14.2.8
- SLT3-PAY-8U-14.2.9

- SLT3-PER-2F-14.3.1
- SLT3-PER-1F-14.3.2
- SLT3-PER-1U-14.3.3

1.3 Block Diagram

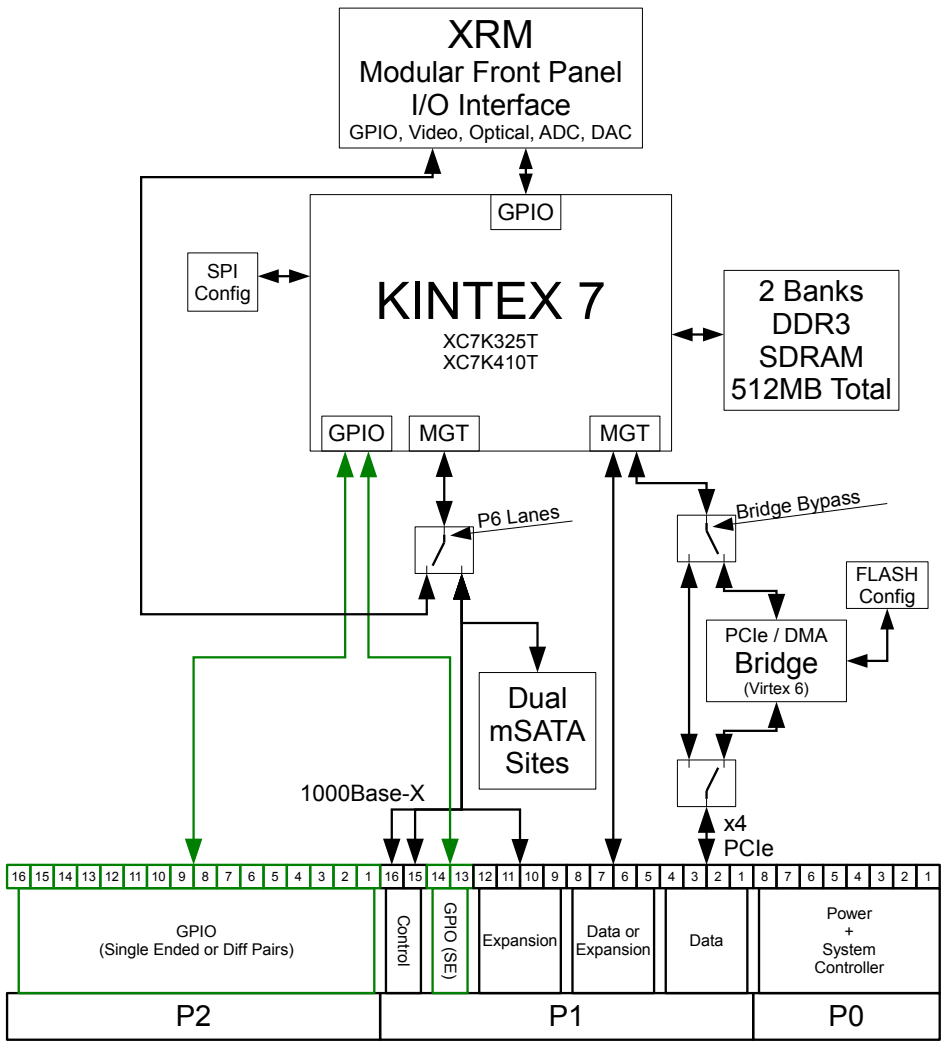

Figure 1 : ADM-XRC-7K1 Block Diagram

Note:
The ADA-VPX3-7K1 is comprised of an ADM-XRC-7K1 XMC card mounted to an ADC-VPX3-XMC VPX carrier specifically designed to host Alpha Data XMCs. All reference to "XMC" refer to the ADM-XRC-7K1, while all references to "Carrier" refer to the ADC-VPX3-XMC.

1.4 Order Code

ADA-VPX3-7K1/z-y(m)(c)(e)

Name	Symbol	Configurations
Kintex-7 Device	z	K325T , K410T
Kintex-7 Speed	y	1 , 2 , 3
Memory	m	blank = Two banks each of 256 MBytes at 1600 MT/s /1 = Two banks of 512 MByte at 800 MT/s
Cooling	c	blank = air cooled commercial /ACE = Extended air cooled commercial /AC1 = air cooled industrial /CC1 = conduction cooled industrial

Table 1 : Build Options

1.5 References and Specifications

ANSI/VITA 42.0	XMC Standard, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.3	XMC PCI Express Protocol Layer Standard, June 2006, VITA, ISBN 1-885731-43-4
ANSI/VITA 46.0	VPX Baseline Standard, October 2007, VITA, ISBN 1-885731-44-2
ANSI/VITA 46.9	PMC/MXC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard, November 2010, VITA, ISBN 1-885731-63-9
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX, July 2010, VITA, ISBN 1-885731-60-4
ANSI/VITA 65	OpenVPX™ System Specification, June 2010, VITA, ISBN 1-885731-58-2
ANSI/IEEE 1386-2001	IEEE Standard for a Common Mezzanine Card (CMC) Family, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	Conduction Cooled PMC, February 2005, VITA, ISBN 1-885731-26-4

Table 2 : References

2 PCB Information

2.1 Physical Specifications

Form Factor	3U VPX
Length	170.6 mm
Width	100.0 mm
Height	17.78 mm
Weigth (air-cooled)	TBD
Weigth (conduction-cooled)	TBD

Table 3 : Physical Specifications

2.2 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.3 System Requirements

The ADA-VPX3-7K1 is a 3U OpenVPX compliant FPGA card with XRM front IO interface. To use the Alpha Data's powerful API and drivers, the system controller must be capable of driving the PCIe lanes to the Bridge. The ADA-VPX3-7K1 also utilizes the OpenVPX 1000Base-X control lines, though this implementation is left to the user.

P2 complies with Vita 46.9 X64S user defined pin configuration with an additional 8 connections to P2 Row G. The X64s can be driven as either 64 single ended signals at 3.3V or 32 differential pairs.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P2 IO and P1 control lanes for use in lab and development environments (Part number: ADC-VPX3-XMC-RTM).

The ADA-VPX3-7K1 can be configured to either utilize 5V or 12V as the main power source. The default build uses 5V, contact sales@alpha-data.com for details on the 12V build option.

2.4 Power Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx™ power estimation tools to determine the exact current requirements for each power rail.

2.5 Headers, Switches and LEDs

2.5.1 Locations

The location of the onboard headers, switches and LEDs are shown in the following sections.

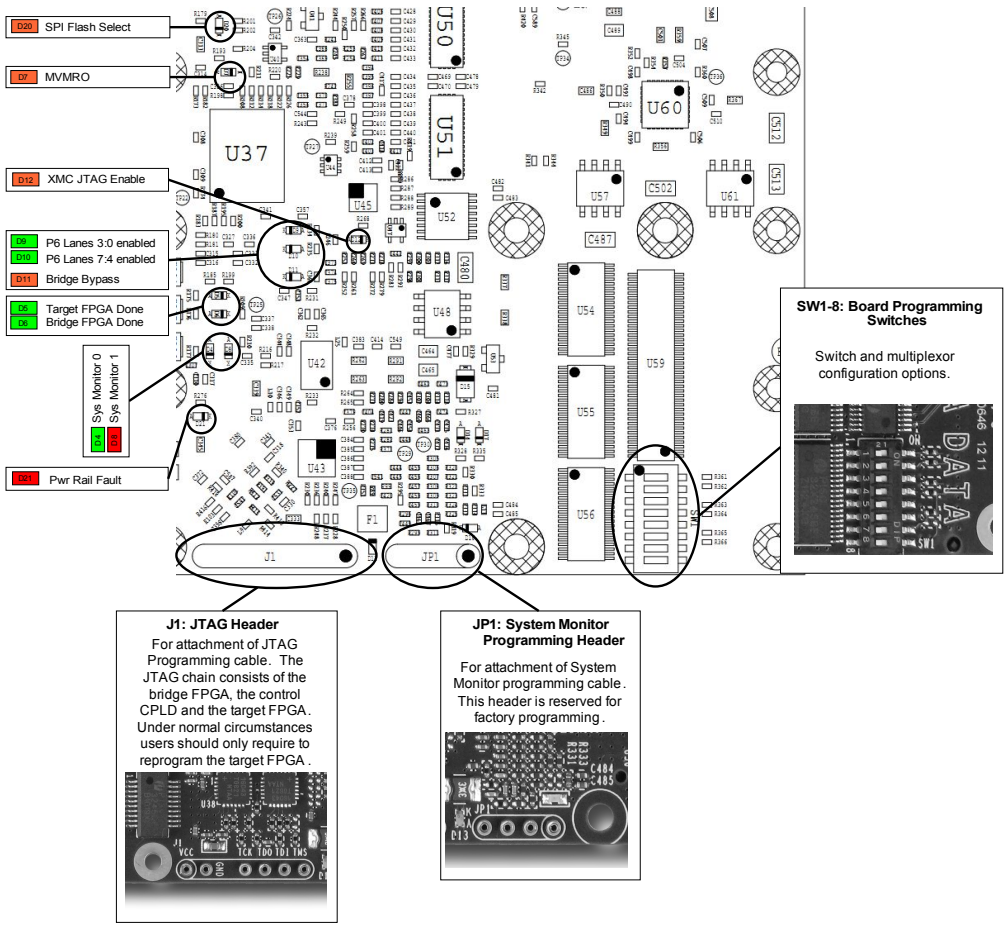

Figure 2 : XMC Headers,Switches and LED Locations

2.5.2 Switch Definitions

Note:
All switches are OFF by default with the exception of Carrier-SW1-2 which must be ON. All Factory Test</ /i> and Reserved switches must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	P6 Lanes (3:0) Enable	Connector P6 lanes (3:0) connected directly to the target FPGA. XRM connector CN2 lanes (3:0) open-circuited.	Connector P6 lanes (3:0) open-circuited. XRM connector CN2 lanes (3:0) connected directly to the target FPGA.
SW1-2	P6 Lanes (7:4) Enable	Connector P6 lanes (7:4) connected directly to the target FPGA. XRM connector CN2 lanes (7:4) open-circuited.	Connector P6 lanes (7:4) open-circuited. XRM connector CN2 lanes (7:4) connected directly to the target FPGA.
SW1-3	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the target FPGA.	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
SW1-4	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
SW1-5	XMC JTAG	Connect JTAG chain to P5.	Isolate JTAG chain from P5.
SW1-6	E-Fuse	Enable E-Fuse programming voltage (VccEFuse = 2.5V).	Disable E-Fuse programming voltage (VccEFuse = 0V).
SW1-7	Systom Monitor Upgrade	Reserved for factory use.	Normal Operation.
SW1-8	SPI Flash Select	Target FPGA configured on power-up by onboard SPI flash device.	Target FPGA configured on power-up by by bridge FPGA.

Table 4 : Switch Definitions

2.5.3 LED Definitions

2.5.3.1 Main LEDs

Comp. Ref.	Function	ON State	Off State
XMC-D4 (Green)	System Monitor Status	See Table 11, "System Monitor Status"	
XMC-D5 (Green)	Bridge FPGA Done	Bridge FPGA is configured	Bridge FPGA is unconfigured
XMC-D6 (Green)	Target FPGA Done	Target FPGA is configured	Target FPGA is unconfigured
XMC-D7 (Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories.
XMC-D8 (Red)	System Monitor Status	See Table 11, "System Monitor Status"	
XMC-D9 (Green)	P6 Lanes (3:0) enabled	P6 Lanes (3:0) enabled. XRM connector CN2 lanes (3:0) disabled	P6 Lanes (3:0) disabled. XRM connector CN2 lanes (3:0) enabled
XMC-D10 (Green)	P6 Lanes (7:4) enabled	P6 Lanes (7:4) enabled. XRM connector CN2 lanes (7:4) disabled	P6 Lanes (7:4) disabled. XRM connector CN2 lanes (7:4) enabled
XMC-D11 (Amber)	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes(3:0) are connected directly to the target FPGA	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
XMC-D12 (Amber)	XMC JTAG	On-board JTAG chain connected to P5	On-board JTAG chain is isolated from P5
XMC-D20 (Amber)	SPI Flash Select	Target FPGA configured on power-up by onboard SPI flash device.	Target FPGA configured on power-up by by bridge FPGA.
XMC-D21 (Red)	Pwr Rail Fault	Power rail fault detected	Power rails operating normally

Table 5 : Main LED Definitions

3 Software Installation

Please refer to the Software Development Kit (SDK) installation CD. The SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

4 Firmware

The **ADA-VPX3-7K1** is equipped with firmware that performs a number of essential on-board tasks, enabling the user to focus on target FPGA application development.

In normal circumstances these devices do not need modification by the board user.

These tasks include power supply sequencing, power supply and temperature monitoring, FPGA configuration and PCIe Endpoint instantiation.

This section provides a brief overview of each item of firmware.

4.1 Bridge FPGA

The bridge FPGA contains a fixed IP design that allows a host system with the Alpha Data ADB3 driver installed to communicate with the board.
API functions provided by the driver allow user applications to perform simple tasks such as configuring the target FPGA and reading sensor information, and also more complex tasks such as DMA transfers.
A complete list of these API functions can be found in the ADMXRC3 API Specification.

4.1.1 PCIe Endpoint

The bridge FPGA is configured on power-up from the onboard flash device. The instantiated bridge design includes a x4 Gen 2 PCIe endpoint routed to lanes (3:0) on connector P5.
A host PCIe system will detect and configure this PCIe endpoint during it's boot process and afterwards hand control of the bridge device to the Alpha Data ADB3 device driver.

4.1.2 Target FPGA Configuration

Running simulataneously to the PCIe endpoint configuration, the bridge FPGA is tasked with configuring the target FPGA, using a group of GPIO pins to the drive the target FPGA's Select Map interface.
In the board's default factory configuration, the bridge configures the target FPGA with the "Simple" FPGA design.
The source code for this design can be found in the ADMXRC Gen 3 SDK.

4.1.3 MPTL Bus

The "Simple" Target FPGA design mentioned in the previous section implements a common block of IP available in the SDK named "mptl_if_target_wrap".
Paired with a corresponding block of IP in the bridge FPGA, this brings up a high-speed serial data channel between the FPGAs: Alpha Data's proprietary Multiplexed Packet Transport Link (MPTL).
Thus, the **ADA-VPX3-7K1** has a ready-made bus capable of 2GB/s data rates in each direction, alleviating from the the user the task of instantiating their own PCIe endpoint, or equivalent, in the target FPGA.

4.1.4 Bridge Bypass Mode

Bridge bypass mode is enabled by setting switch XMC-SW1-3 to the ON position. In this mode, lanes (3:0) on connector P1 are routed directly to the target FPGA.
Combined with lanes (7:4), which are always routed directly to the target FPGA, the user can instantiate a x8 PCIe endpoint in the target FPGA.

Note that whilst in Bridge Bypass mode, the bridge FPGA will still configure the target FPGA on power-up, provided switch SW1-8 (SPI Flash select) and SW1-4 (Flash Boot Inhibit), are both in the OFF position.

4.2 Flash Memory

A 512Mb Flash Memory (Intel / Numonyx PC28F512P30EF) is used to store the configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible via the Bridge FPGA using API functions.

Utilities for erasing, programming and verification of the flash memory, which implement these API functions, are provided in the ADM-XRC Gen 3 SDK.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED D7, as shown in Figure XMC Headers,Switches and LED Locations.

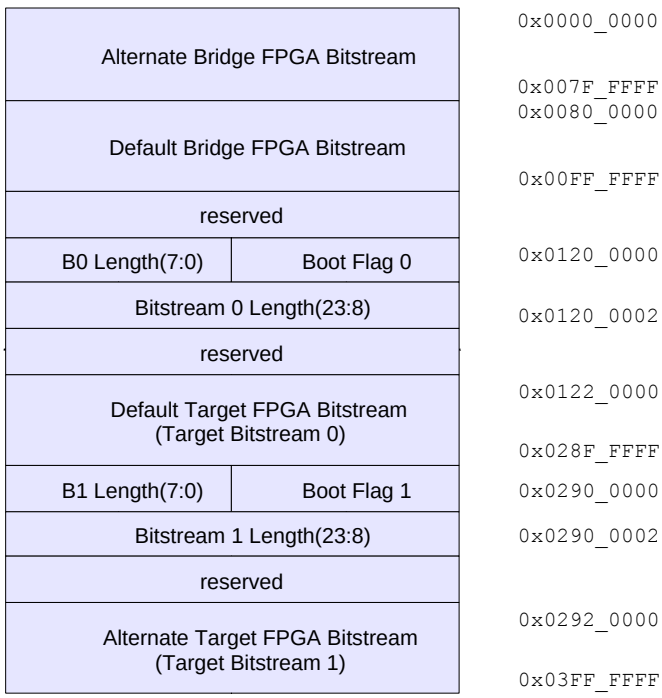

Figure 3 : Flash Memory Map

4.3 System Monitor

The **ADA-VPX3-7K1** has an onboard Atmel AVR microcontroller (uC) used for system monitoring.

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the bridge FPGA.

The following voltage rails and temperatures are monitored by the microcontroller:

Voltage Rail	Description
VPWR	Board Input Supply (either 5.0V or 12.0V)
12.0V	Internally generated 12V Supply
5.0V	Internally generated 5V supply
3.3V	Board Input Supply
2.5V	Bridge and Target FPGA VCCO/VCCAUX
2.0V	Target FPGA VCC AUX IO
1.8V	Flash Memory
1.8V	Target FPGA MGT AVCC AUX
1.5V	DDR3 SDRAM, Target FPGA memory I/O
Variable	Target FPGA XRM VCCO
1.0V	Bridge and Target FPGA VCC INT
1.2V	Target FPGA MGT AVTT
1.2V	Target FPGA MGT AVCC
1.2V	Bridge FPGA MGT AVCC

Table 6 : Voltage Rails Monitored by Microcontroller

Temperature Monitor Point
Microcontroller internal temperature
TMP421 internal temperature
Bridge FPGA on-die temperature (measured in TMP421)
Target FPGA on-die temperature (measured in TMP421)

Table 7 : Temperatures Monitored by Microcontroller

In addition, the following voltage rails and temperatures are monitored by a Xilinx™ System Monitor block within the FPGA:

Voltage Rail	Description
1.0V	FPGA VCC INT
2.5V	FPGA VCC AUX

Table 8 : Voltage Rails Monitored by Bridge FPGA

Temperature Monitor Point
Bridge FPGA on-die temperature

Table 9 : Temperatures Monitored by Bridge FPGA

The SDK includes two example applications ("sysmon" and "monitor") that read the system monitor sensor values.

4.3.1 Automatic Over-Temperature Protection

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is within 10 \dC of the upper or lower limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5\dC margin to prevent measurement errors triggering a false alarm.

	FPGAs (Bridge and Target)				Board (uC and PCB)			
	Min	Lower Warning	Upper Warning	Max	Min	Lower Warning	Upper Warning	Max
Commercial	-5 degC	+5 degC	+80 degC	+90 degC	-5 degC	+5 degC	+80 degC	+90 degC
Extended	-5 degC	+5 degC	+95 degC	+105 degC	-5 degC	+5 degC	+95 degC	+105 degC
Industrial	-45 degC	-35 degC	+95 degC	+105 degC	-45 degC	-35 degC	+95 degC	+105 degC

Table 10 : Temperature Limits

4.3.2 System Monitor Status LEDs

Status	D4 (Green)	D8 (Amber)
Standby (3V3 Aux Only)	On	On
Running and No Alarms	On	Off
Warning - temperature reading approaching limit or supply rail out of range	Blink	On
Critical Countdown - temperature reading out of range - target FPGA due to be cleared	Blink	Blink
Critical temperature reading out of range - target FPGA has been cleared	Off	Blink
Factory Programming Mode	Blink (Alternating)	Blink (Alternating)

Table 11 : System Monitor Status

4.4 Control CPLD

A Xilinx™ XC2C64A CPLD appears in the JTAG chain along with the bridge and target FPGAs. This is used for propagating DIP switch settings to the onboard devices, LED driving and level translation.

4.5 IPMI EEPROM

A 4 Kbit I2C EEPROM (type M24C04) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

5 Target FPGA

5.1 Target FPGA Characteristics

The ADA-VPX3-7K1 supports Kintex-7 K325T and K410T devices in the FFG900 and FBG900 package. The distinguishing characteristics of these devices are described in table Target FPGA Characteristics. These figures are taken from the Kintex-7 FPGA Feature Summary available in the Xilinx™ Kintex-7 datasheet. The maximum user I/O does not change with device selected and is split between the P5, P6 and XRM external connectors, the onboard memory, the Ethernet PHY and the Bridge FPGA links.

Device	Logic Cells	Slices	Distributed RAM	DSP Slices	Block RAM	CMTs	PCIe Hard Macros
XC7K325T	326,080	50,950	4,000 Kb	840	16,020 Kb	10	1
XC7K410T	406,720	63,550	5,663 Kb	1,540	28,620 Kb	10	1

Table 12 : Target FPGA Characteristics

5.2 IO Bank Utilisation

The layout of the target FPGA's I/O banks are shown in Figure IO Banks.

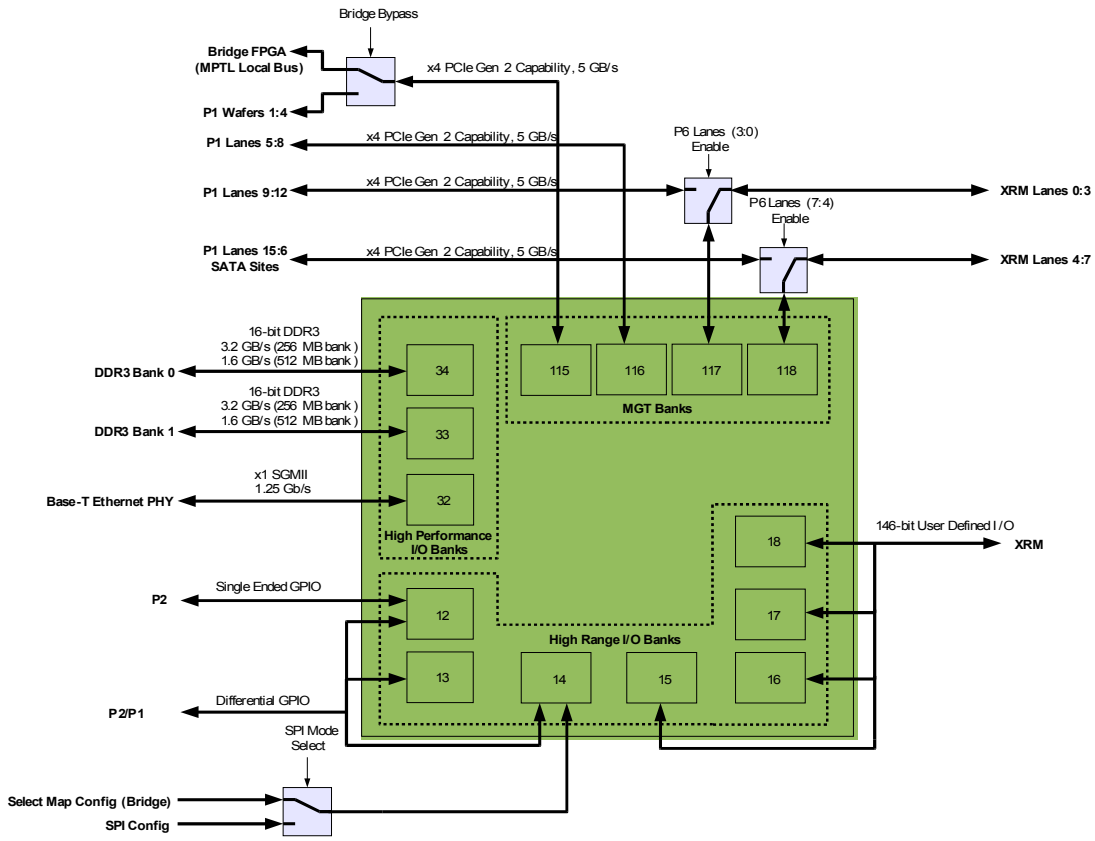

Figure 4 : IO Banks

The Kintex-7 FPGA has three distinct types of I/O banks: MGT banks, High-Range banks and High-Performance banks.

The compatible I/O standards vary between each type of bank. *The Xilinx™ 7 Series FPGAs SelectIO Resources user guide should be consulted for further information.* The sections that follow describe how the banks are divided between the onboard features and external connectors.

5.2.1 MGT Banks

The ADA-VPX3-7K1's target FPGA has four MGT banks, each containing four transceivers.

The four transceivers in Bank 115 are normally routed to the bridge FPGA forming the onboard MPTL bus, but can be routed directly to connector P1 wafers (1:4) by moving switch SW1-3 to the ON position, enabling Bridge Bypass Mode.

The four transceivers in Bank 116 are routed to connector P1 wafers (5:8).

The four transceivers in Bank 117 are normally routed to connector XRM lanes (0:3), but can be routed instead to P1 lanes (9:12) by moving switch SW1-1 to the ON position.

The four transceivers in Bank 118 are normally routed to connector XRM lanes (4:7), but can be routed instead to P1 wafers (15:16) and the two integrated mSATA sites by moving switch XMC-SW1-2 to the ON position.

XRM Lanes (0:6) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

The complete MGT pin mapping is shown in Rear MGT Connections to the Target FPGA.

5.2.2 High Performance I/O Banks

The high performance I/O banks are used with the onboard DDR3 Memory and Gigabit Ethernet devices.

5.2.2.1 DDR3 Memory

As shown in Figure IO Banks the ADA-XRC-7K1 has two independent banks of DDR3 SDRAM. Each bank consists of one memory device with a 16-bit wide datapath.
Two memory configurations are available: banks with a capacity of 2 Gb capable of running at 800 MHz (1600 Mb/s) or banks with a capacity of 4 Gb capable of running at 400 MHz (800 Mb/s).

FPGA Banks 33 and 34 each provide an interface to one memory bank/device. For maximum pin utilisation, the 200MHz reference clocks for each memory bank are routed into the FPGA through the adjacent bank 32.
As exemplified in the constraints files contained in the ADMXRC3 SDK for the ADA-VPX3-7K1, bank 32 must also be used to cascade DCI to banks 33 and 34.

The trade-off between memory capacity and transfer rate is determined by how the Vref I/O pins on the FPGA are utilised.
The memory interfaces use stub-series transceiver logic (SSTL) which is a single-ended I/O standard with a differential input buffer. The reference voltage for the differential buffer is normally generated outside of the FPGA and supplied through
the Vref I/O pins. However, when the user chooses to generate Vref internally, two I/O pins are freed up: one of which can be used for an extra address line to the memory devices, allowing 4Gb devices to be used. The compromise is that using internal VREF limits the transfer rate to 400 MHz (800Mb/s).

The memory banks are arranged for compatibility with the Xilinx™ Memory Interface Generator (MIG). Full details of the interface, signaling standards and an example design are provided in the SDK.

5.2.3 High Range I/O Banks

The high range I/O banks are used for GPIO between the FPGA and three of the external connectors: the XRM front panel interface and VPX connectors P1 and P2.

5.2.3.1 P1 and P2 GPIO

There are 72 GPIO signals routed between connector P1/P2 and high range banks.

All of these signals are routed differentially and can therefore can be used as single-ended signals or as differential pairs.

Whilst the I/O voltage for the FPGA banks are fixed at 2.5V, level translating quick switches between the FPGA and VPX connectors ensure compatibility with both 3.3V and 2.5V signalling levels.

The complete P1 and P2 GPIO pinout is shown in A.3.

5.2.3.2 XRM GPIO

The XRM general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA, with each group routed to an invidual high range bank. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that can be 2.5V, 1.8V, 1.5V or 1.2V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	18	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	17	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	16	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	15	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 13 : XRM GPIO Groups

The complete XRM pinout is shown in B.

5.3 Clocks

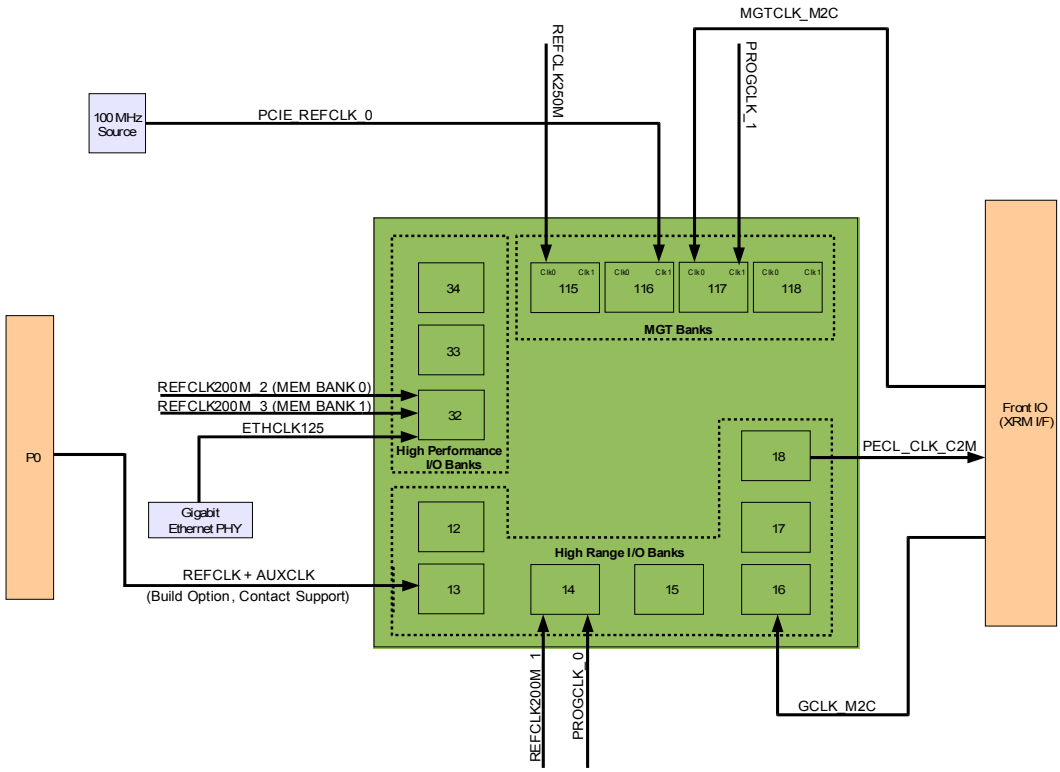

Figure 5 : Clocks

5.3.1 200MHz Reference Clock (REFCLK200M)

The fixed 200MHz reference clock "REFCLK200M" is a differential clock signal using LVDS. This signal is widely distributed throughout the board.

It is distributed to the bridge FPGA, Bank 14 of the Target FPGA and to two places on Bank 32 of the Target FPGA.

Both branches of the clock at bank 32 are intended for use with the memory interfaces. They are converted to HSTL for compatibility with the I/O voltage of the bank.

This clock can be used to generate application-specific clock frequencies using the PLLs within the FPGA. It is also suitable as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK200M_1	200 MHz	IO_L11_T1_MRCC_14	LVDS	T26	T27
REFCLK200M_2	200 MHz	IO_L12_T1_MRCC_32	HSTL_I	AF17	AG17
REFCLK200M_3	200 MHz	IO_L13_T1_MRCC_32	HSTL_I	AD18	AE18

Table 14 : REFCLK200M Connections

5.3.2 250MHz Reference Clock (REFCLK250M)

The reference clock "REFCLK250" is a differential clock generated onboard and is intended for use with the MPTL local bus link to the bridge FPGA.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK250	250 MHz	MGTREFCLK0_115	LVDS	R8	R7

Table 15 : REFCLK250 Connections

5.3.3 PCIe Reference Clock 0 (PCIEREFCLK0)

The 100MHz PCI Express reference clock "PCIEREFCLK0" is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This clock is buffered into two PCI Express reference clocks that are forwarded to the Bridge and Target FPGA respectively.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK0	100 MHz	MGTREFCLK1_116	LVDS	N8	N7

Table 16 : PCIEREFCLK0 Connections

5.3.4 AUXCLK

Auxiliary Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for 1PPS synchronization signaling. This clock is not connected by default and must be added as a build option. Contact Alpha-Data Support for details.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
1PPS or AUXCLK	IO_L22P/N_T3_13	LVDS	AH26	AH27

Table 17 : AUXCLK Connections

5.3.5 REFCLK COnnections

Ref Clock. This clock is a direct input to the target FPGA. In OpenVPX this clock line is used for system clock syncronization. This clock is not connected by default and must be added as a build option. Contact Alpha-Data Support for details.

Signal	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK	O_L15P/ N_T2_DQS_13	LVDS	AK29	AK30

Table 18 : AUXCLK Connections

5.3.6 Programmable Clocks (PROGCLK0:1)

There are two user-programable clocks using LVDS. These clocks are programmable through the Alpha Data ADM-XRC Gen 3 SDK. "PROGCLK0" is generated in the Bridge FPGA by the the Alpha Data ADB3 driver and offers a less accurate frequency resolution, but with a wider programmable frequency range. "PROGCLK1" is generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK0	5 - 700 MHz	IO_L13_T2_MRCC_14	LVDS	U27	U28
PROGCLK1	5 - 312.5 MHz	MGTREFCLK1_117	LVDS	J8	J7

Table 19 : PROGCLK Connections

5.3.7 Module-Carrier Global Clock (GCLK_M2C)

The clock "GCLK_M2C" is a differential clock signal using LVDS. It is provided by an XRM module through the XRM connector, CN1, at pins 110 & 108. It is connected to an MRCC input on the Target FPGA.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
GCLK_M2C	Variable	IO_L13_T2_MRCC_16	LVDS	D27	C27

Table 20 : GCLK_M2C Connections

5.3.8 Module-Carrier MGT Clock (MGTCLK_M2C)

The reference clock "MGTCLK_M2C" is a differential clock signal using LVDS. The clock is provided by an XRM module through the XRM connector, CN1, at pins 109 & 111. It is connected to MGT Bank 117 on the Target FPGA for application specific frequencies / line rates.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK_M2C	Variable	MGTREFCLK0_117	LVDS	G8	G7

Table 21 : MGTCLK_M2C Connections

5.3.9 Carrier-Module PECL Clock (PECL_CLK_C2M)

The clock "PECL_CLK_C2M" is a differential clock signal using 2.5V PECL levels. The clock is provided by the target FPGA and connected to an XRM module through the XRM connector, CN1, at pins 113 & 115.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PECL_CLK_C2M	Variable	IO_L12_T1_MRCC_18	PECL	G13	F13

Table 22 : PECL_CLK_C2M Connections

5.4 Configuration

5.4.1 JTAG

A JTAG boundary scan chain is connected to header XMC-J1. This allows the connection of the Xilinx™ JTAG cable for FPGA configuration and debug using the appropriate Xilinx™ tools.

The JTAG Header pinout is shown in Figure JTAG Header XMC-J1:

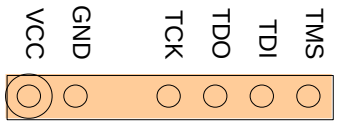

Figure 6 : JTAG Header XMC-J1

The scan chain is shown in Figure JTAG Boundary Scan Chain:

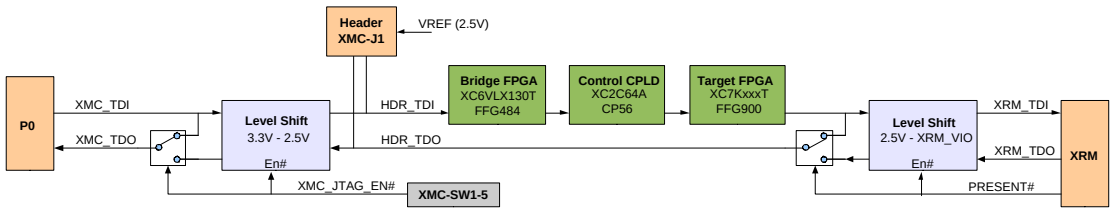

Figure 7 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the XMC connector (switch XMC-SW1-5 is ON), Header XMC-J1 should not be used.

5.4.2 Select Map (via the Bridge FPGA)

The target FPGA can be configured through its Select Map interface on bank 14. The select map interface is connected to the bridge FPGA and it is through this that the target FPGA can be configured.

At power up, if valid data is stored in the flash memory the bridge will automatically configure the Target FPGA. This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch, Switch XMC-SW1-4 to ON.

The target FPGA may also be configured/reconfigured at any time by invoking an ADMXRC3 API function on a host machine with the Alpha Data ADB3 Device Driver installed.

5.4.3 Quad SPI Flash

TBD

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Appendix A: VPX Connector Pinouts

Appendix A.1: P0 Signal Description

Pin Name	Direction	Description
VPWR	-	Supply Rail. May be 12.0V or 5.0V
3V3	-	3.3V Supply Rail
5V0	-	5.0V Supply Rail
12V0	-	12.0V Supply Rail
3V3_AUX	-	3.3V Auxiliary Supply Rail. This rail is used for onboard monitoring circuits. If this rail isn't supplied by the carrier a resistor fit option allows the monitoring circuits to be supplied by 3.3V
AUXCLK	In	OpenVPX 1PPS backplane synchronization clock
MSCL	In	IPMI I2C serial clock
MSDA	In	IPMI I2C serial data
GA(4:0) and GAP	In	VPX slot address
MVMRO	In	XMC Write Prohibit. This signal is an input from the carrier. When asserted (high) , all writes to non-volatile memories are inhibited. This is indicated by the Amber LED , D7.
SYSRESET/		In
TRST_L	In	JTAG reset
TCK	In	JTAG clock
TMS	In	JTAG mode select
TDI	In	JTAG test data in
TDO	Out	JTAG test data out

Table 23 : P0 Signal Description

Appendix A.2: Rear MGT Connections to the Target FPGA

Signal	TGT FPGA + Pin	TGT FPGA - Pin	VPX Connector + Pin	VPX Connector - Pin
MPTL_T2B<0>/ PCIE_TX<0>	Y2	Y1	P1.D1	P1.E1
MPTL_T2B<1>/ PCIE_TX<1>	V2	V1	P1.E2	P1.F2
MPTL_T2B<2>/ PCIE_TX<2>	U4	U3	P1.D3	P1.E3
MPTL_T2B<3>/ PCIE_TX<3>	T2	T1	P1.E4	P1.F4
PCIE_TX<4>	L4	L3	P1.D5	P1.E5
PCIE_TX<5>	M2	M1	P1.E6	P1.F6
PCIE_TX<6>	N4	N3	P1.D7	P1.E7
PCIE_TX<7>	P2	P1	P1.E8	P1.F8
P6_TX<0>/XRM_C2M<0>	K2	K1	P1.D9	P1.E9
P6_TX<1>/XRM_C2M<1>	J4	J3	P1.E10	P1.F10
P6_TX<2>/XRM_C2M<2>	H2	H1	P1.D11	P1.E11
P6_TX<3>/XRM_C2M<3>	F2	F1	P1.E12	P1.F12
P6_TX<4>/XRM_C2M<4>	D2	D1	P1.D15	P2.E15
P6_TX<5>/XRM_C2M<5>	C4	C3	P1.E16	P1.F16
P6_TX<6>/XRM_C2M<6>	B2	B1	SATA_0	SATA_0
P6_TX<7>/XRM_C2M<7>	A4	A3	SATA_1	SATA_1
-	-	-	-	-
MPTL_T2B<0>/ PCIE_RX<0>	AA4	AA3	P1.A1	P1.B1
MPTL_T2B<1>/ PCIE_RX<1>	Y6	Y5	P1.B2	P1.C2
MPTL_T2B<2>/ PCIE_RX<2>	W4	W3	P1.A3	P1.B3
MPTL_T2B<3>/ PCIE_RX<3>	V6	V5	P1.B4	P1.C4
PCIE_RX<4>	M5	M6	P1.A5	P1.B5
PCIE_RX<5>	P6	P5	P1.B6	P1.C6
PCIE_RX<6>	R4	R3	P1.A7	P1.B7
PCIE_RX<7>	T6	T5	P1.B8	P1.C8
P6_RX<0>/XRM_M2C<0>	K6	K5	P1.A9	P1.B9
P6_RX<1>/XRM_M2C<1>	H6	H5	P1.B10	P1.C10
P6_RX<2>/XRM_M2C<2>	G4	G3	P1.A11	P1.B11

Table 24 : Rear MGT Connections to the Target FPGA (continued on next page)

Signal	TGT FPGA + Pin	TGT FPGA - Pin	VPX Connector + Pin	VPX Connector - Pin
P6_RX<3>/XRM_M2C<3>	F6	F5	P1.B12	P1.C12
P6_RX<4>/XRM_M2C<4>	E4	E3	P1.A15	P1.B15
P6_RX<5>/XRM_M2C<5>	D6	D5	P1.B16	P1.C16
P6_RX<6>/XRM_M2C<6>	B6	B5	SATA_0	SATA_0
P6_RX<7>/XRM_M2C<7>	A8	A7	SATA_1	SATA_1

Table 24 : Rear MGT Connections to the Target FPGA

Appendix A.3: GPIO Connections to the Target FPGA

Signals beginning with GP can operate as single ended or differential. These signals pass through a FET bus switch. By limiting the signal voltage at 2.5V, these allow the use of 3.3V or 2.5V signalling levels to be used.

Signals beginning with SE are single ended. These signals pass through a FET bus switch. By limiting the signal voltage at 2.5V, these allow the use of 3.3V or 2.5V signalling levels to be used.

Signal	VPX Connector. Pin	Target FPGA	|	Target FPGA	VPX Connector. Pin	Signal
GP1_P	P2.E1	AA25	|	AB25	P2.D1	GP1_N
GP2_P	P2.B1	AD29	|	AE29	P2.A1	GP2_N
GP3_P	P2.F2	W29	|	Y29	P2.E2	GP3_N
GP4_P	P2.C2	Y28	|	AA28	P2.B2	GP4_N
GP5_P	P2.E3	AA22	|	AA23	P2.D3	GP5_N
GP6_P	P2.B3	Y23	|	Y24	P2.A3	GP6_N
GP7_P	P2.F4	AC26	|	AD26	P2.E4	GP7_N
GP8_P	P2.C4	Y21	|	AA21	P2.B4	GP8_N
GP9_P	P2.E5	AH26	|	AH27	P2.D5	GP9_N
GP10_P	P2.B5	AD27	|	AD28	P2.A5	GP10_N
GP11_P	P2.F6	AE28	|	AF28	P2.E6	GP11_N
GP12_P	P2.C6	AF26	|	AF27	P2.B6	GP12_N
GP13_P	P2.E7	AC20	|	AC21	P2.D7	GP13_N
GP14_P	P2.B7	AG27	|	AG28	P2.A7	GP14_N
GP15_P	P2.F8	AJ27	|	AK28	P2.E8	GP15_N
GP16_P	P2.C8	AJ26	|	AK26	P2.B8	GP16_N
GP17_P	P2.E9	Y26	|	AA26	P2.D9	GP17_N
GP18_P	P2.B9	AB22	|	AB23	P2.A9	GP18_N
GP19_P	P2.F10	AA27	|	AB28	P2.E10	GP19_N
GP20_P	P2.C10	AG29	|	AH29	P2.B10	GP20_N
GP21_P	P2.E11	AJ28	|	AJ29	P2.D11	GP21_N
GP22_P	P2.B11	AB27	|	AC27	P2.A11	GP22_N

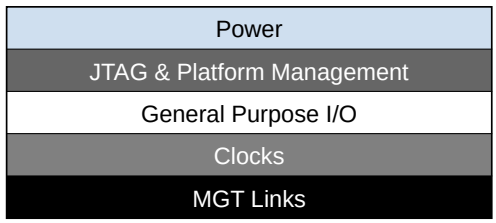
Table 25 : VPX GPIO Signals (continued on next page)

Signal	VPX Connector. Pin	Target FPGA		Target FPGA	VPX Connector. Pin	Signal
GP23_P	P2.F12	AG30	|	AH30	P2.E12	GP23_N
GP24_P	P2.C12	AK29	|	AK30	P2.B12	GP24_N
GP25_P	P2.E13	AC29	|	AC30	P2.D13	GP25_N
GP26_P	P2.B13	AE30	|	AF30	P2.A13	GP26_N
GP27_P	P2.F14	Y30	|	AA30	P2.E14	GP27_N
GP28_P	P2.C14	AB29	|	AB30	P2.B14	GP28_N
GP29_P	P2.E15	W27	|	W28	P2.D15	GP29_N
GP30_P	P2.B15	V25	|	W26	P2.A15	GP30_N
GP31_P	P2.F16	V19	|	V20	P2.E16	GP31_N
GP32_P	P2.C16	U22	|	U23	P2.B16	GP32_N
GP1	P2.G1	AE23	|	AG20	P2.G3	GP2
GP3	P2.G5	AF23	|	AH20	P2.G7	GP4
GP5	P2.G9	AF20	|	AA20	P2.G11	GP6
GP7	P2.G13	AF21	|	AB20	P2.G15	GP8
GP9	P1.E14	AB24	|	AD21	P1.B14	GP10
GP11	P1.F14	AC25	|	AE21	P1.C14	GP12
GP13	P1.D13	AC24	|	AC22	P1.A13	GP14
GP15	P1.E13	AD24	|	AD22	P1.B13	GP16

Table 25 : VPX GPIO Signals

Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general-purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



Appendix B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	J12	1	2	L13	DA_N1
DA_P0	J11	3	4	L12	DA_P1
DA_N2	J13	5	6	K14	DA_P3
DA_P2	K13	7	8	J14	DA_N3
DA_N4	H12	9	10	E15	DA_N5
DA_P4	H11	11	12	E14	DA_P5
DA_N6	E11	13	14	D13	DA_N7
DA_P6	F11	15	16	D12	DA_P7
DA_P8	F12	17	18	J16	DA_P9
DA_N8	E13	19	20	H16	DA_N9
DA_N10	B12	21	22	A12	DA_N11
DA_P10	C12	23	24	A11	DA_P11
DA_N12	C11	25	26	L16	DA_P13
DA_P12	D11	27	28	K16	DA_N13
DA_N14	K15	29	30	H15	DA_P15
DA_P14	L15	31	32	G15	DA_N15
DB_N0	H22	33	34	F22	DB_N1
DB_P0	H21	35	36	G22	DB_P1
SA_0	G12	37	38	H14	
3V3	-	39	40	G14	
3V3	-	41	42	-	
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
	-	55	56	-	
	-	57	58	-	
	-	59	60	-	

Table 26 : XRM Connector CN1, Field 1

Appendix B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	D18	61	62	L18	DB_N3
DB_P2	D17	63	64	L17	DB_P3
DB_N4	F17	65	66	H19	DB_N5
DB_P4	G17	67	68	J19	DB_P5
DB_N6	B17	69	70	J18	DB_N7
DB_P6	C17	71	72	K18	DB_P7
DB_N8	C16	73	74	H20	DB_P9
DB_P8	D16	75	76	G20	DB_N9
DB_P10	F21	77	78	H17	DB_N11
DB_N10	E21	79	80	J17	DB_P11
DB_N12	C21	81	82	E19	DB_P13
DB_P12	D21	83	84	D19	DB_N13
DB_N14	C22	85	86	F18	DB_N15
DB_P14	D22	87	88	G18	DB_P15
	F20	89	90	E18	SB_1
	E20	91	92	F23	SC_0
SA_1	F16	93	94	G25	SC_1
SB_0	G19	95	96	M19	SD_0
	C25	97	98	A23	DC_N1
	B25	99	100	B23	DC_P1
DC_N0	D24	101	102	L25	
DC_P0	E24	103	104	K25	
SD_1	P19	105	106	N22	SD_3
SD_2	N21	107	108	D27	
	G8	109	110	C27	
	G7	111	112	-	
	F13	113	114	-	
	G13	115	116	-	
	A4	117	118	A8	
	A3	119	120	A7	

Table 27 : XRM Connector CN1, Field 2

Appendix B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	D29	121	122	C24	DC_P3
DC_N2	C30	123	124	B24	DC_N3
DC_N4	C26	125	126	B27	DC_P5
DC_P4	D26	127	128	A27	DC_N5
DC_P6	E28	129	130	A25	DC_P7
DC_N6	D28	131	132	A26	DC_N7
DC_N8	B29	133	134	A30	DC_N9
DC_P8	C29	135	136	B30	DC_P9
DC_P10	F26	137	138	A28	DC_N11
DC_N10	E26	139	140	B28	DC_P11
DC_P12	E29	141	142	F28	DC_N13
DC_N12	E30	143	144	G28	DC_P13
DC_N14	E25	145	146	L21	DD_P1
DC_P14	F25	147	148	K21	DD_N1
DD_P0	K26	149	150	D23	DC_N15
DD_N0	J26	151	152	E23	DC_P15
DD_P2	L26	153	154	J22	DD_N3
DD_N2	L27	155	156	J21	DD_P3
DD_N4	H29	157	158	J28	DD_N5
DD_P4	J29	159	160	J27	DD_P5
DD_P6	M28	161	162	L23	DD_N7
DD_N6	L28	163	164	L22	DD_P7
DD_N8	K30	165	166	K29	DD_N9
DD_P8	L30	167	168	K28	DD_P9
DD_N10	N30	169	170	J24	DD_N11
DD_P10	N29	171	172	J23	DD_P11
DD_N12	M27	173	174	M30	DD_N13
DD_P12	N27	175	176	M29	DD_P13
DD_N14	N26	177	178	K24	DD_N15
DD_P14	N25	179	180	K23	DD_P15

Table 28 : XRM Connector CN1, Field 3

Appendix B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
	K2	1	2	K6	
	K1	3	4	K5	
	J4	5	6	H6	
	J3	7	8	H5	
	D2	9	10	E4	
	D1	11	12	E3	
	C4	13	14	D6	
	C3	15	16	D5	
	H2	17	18	G4	
	H1	19	20	G3	
	F2	21	22	F6	
	F1	23	24	F5	
	B2	25	26	B6	
	B1	27	28	B5	

Table 29 : XRM Connector CN2

Revision History

Date	Revision	Changed By	Nature of Change
23 Oct 2012	0.1	K. Roth	Initial Draft
6 Feb 2013	1.0	K. Roth	Initial Release
1 Aug 2014	2.0	K. Roth	Amended description of XRM_VIO in Section 5.2.3.2

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